

REMARKS

Applicant thanks the Examiner for indication that claim 1 contains allowable subject matter related to the FET with a dual-gate with polysilicon gate regions having silicide sidewalls formed thereon.

Claims 1 to 8 and 18 to 22 remain active in this application. By the present amendment claims 1, 5, 7, 8, 18, 19 and 22 have been amended responding to the Examiner's objection-rejection. The support for the present amendment can be found in at least Figure 2 and paragraphs 0010 and 0023 of the present specification. No new matter is introduced by this amendment.

Claims 7, 8, 19 and 22 have been objected to because of the number of informalities. Specifically, in claim 7 the word "damascene" is doubled. In claims 18 and 19 the word "recited" is missed when reference to the preceding claim is done. Additionally, in claim 22 an article in front of "shallow trench isolation structure" is omitted.

Responding to these objections claims 7, 8, 19 and 22 have been amended to correct all above described issues. The Examiner is respectfully requested to withdraw the objections to the claims in view of the present amendment.

Claims 1 to 8 and 18 to 22 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner refers to the term "a first thickness of the conduction channel". The Examiner finds the meaning of the term "thickness" unclear in much the same manner as the Examiner previously criticized the term "width" for which "thickness" was substituted in an effort to satisfy the Examiner. Responding to this rejection claim 1 has been amended to avoid use of either of these terms by use of a structurally descriptive phrase using the term "dimension".

The issue with the term "a first width" has been existing in the application from the very beginning of prosecution. Since double-gate structures can be confusing because of the rotated structures as compared with conventional FETs. Specifically, a monocrystalline region of a transistor would have length (in the

direction of carrier flow and parallel to the gates/dielectrics), width (perpendicular to carrier flow, but parallel to the gates/dielectrics) and thickness (perpendicular to carrier motion, and perpendicular to the two gates/dielectrics). In the previous amendments the term “first width” has been also presented as “thickness”. The Examiner still finds all these terms confusing. In the present amendment the term “first thickness” was replaced with a term “dimension”. Specifically, claim 1 as presently amended recites, “A field effect transistor with a dual-gate, comprising:

a monocrystalline conduction channel dual-gate wherein gate electrode portions are separated across said monocrystalline conduction channel by a dimension of 100nm or less,...” (Emphases added)

Applicant believes that this amendment makes the claimed structure abundantly clear and at the same time maintains the standard FET nomenclature. The Examiner is respectfully requested to reconsider the application in view of the present amendment and allow the application.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 1 to 8 and 18 to 22 be allowed, and that the application be passed to issue.

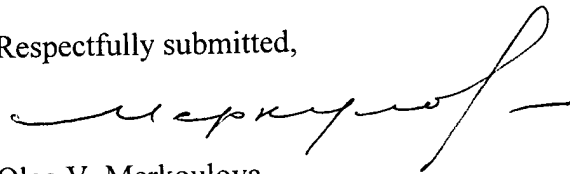
Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

Docket BUR919990299
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A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456 of International Business Machines Corporation (Burlington).

Respectfully submitted,



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